AK2364

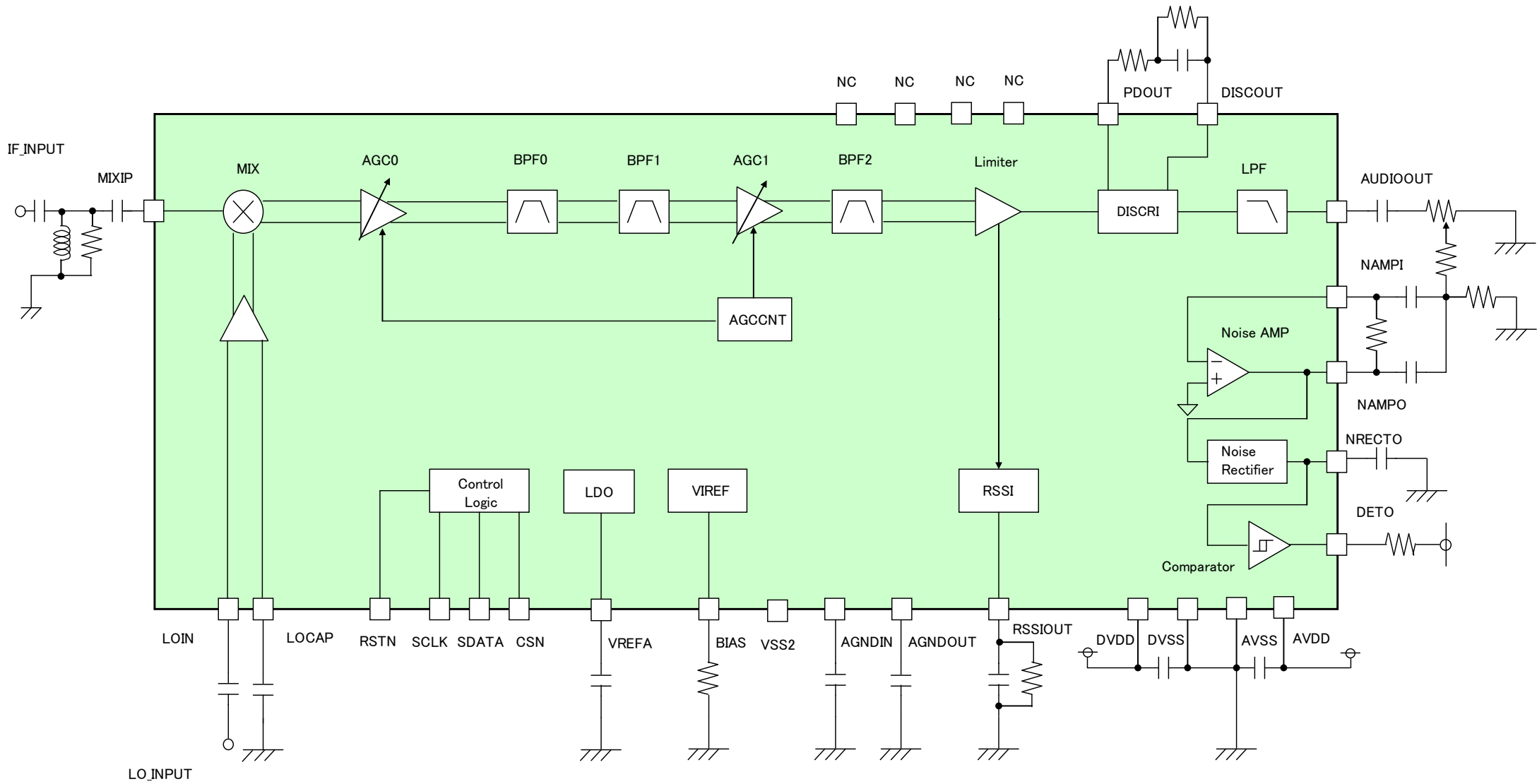## Two-way Radio Filterless FM Detector LSI

1. Features

The AK2364 includes 2nd-Mixer, AGC+BPF, PLL FM detector, noise squelch, and RSSI circuit. This device can eliminate D to G type ceramic filters, quadrature discriminator, and other external components.

• Low operating voltage: VDD = 2.6 to 5.5 V
• Wide operating temperature: Ta = -40 to 85 °C
• Hi sensitivity: -104dBm at 12dB SINAD
• Built-in 2nd Mixer
• Local frequency: 45.9MHz, 50.4MHz, 57.6MHz (Triple of 15.3, 16.8 and 19.2MHz)
• Built-in programmable AGC+BPF circuits corresponding to D to G type ceramic filters
• Built-in PLL FM detector
• RSSI function
• Built-in noise squelch circuits
• Low consumption current: 7mA
• Compact plastic packaging, 28-pin QFNJ （4.0 x 4.0 x 0.75mm, 0.4mm pitch）

2. Contents

3. Block Diagram

4. Circuit Configuration

Block	Description
MIX	2nd-mixer to convert the input signal down to 450Hz.
AGC+BPF	The circuit composed of AGC and BPF, where the desired signal is amplified and spurious components included in the signal from the 2nd-mixer are eliminated.
Divider	The circuit to divide the signal from LOIN pin and supply BPF with CLK.
LIMTER	The circuit to amplify the signal filtered at the AGC+BPF stage and generate rectangular wave.
DISCRI	The demodulator circuit with PLL FM detector, where the audio signal is recovered.
LPF	The Low-pass filter to eliminate the noise generated at the DISCRI stage.
Noise AMP	The amplifier to compose the Band-pass filter for noise squelch.
Noise Rectifier	The rectification circuit to detect the noise level.
Comparator	The circuit to compare the noise level with reference voltage level.
RSSI	The circuit to indicate the Received Signal Strength Indicator(RSSI) by generate a DC voltage corresponding to the input level from LIMITER.
VIREF	The circuit to generate internal reference voltage.
LDO	The circuit to supply 1.8V power for some circuits.
Control Logic	The control register controls the status of internal condition by serial data that consists of 1 instruction bit, 6 address bits and 8 data bits.

Note: When you use AK2364 in AVDD=2.6 to 3.6V operation, VREFA pin is connected to AVDD pin for power supplying.

5. Pin/Function

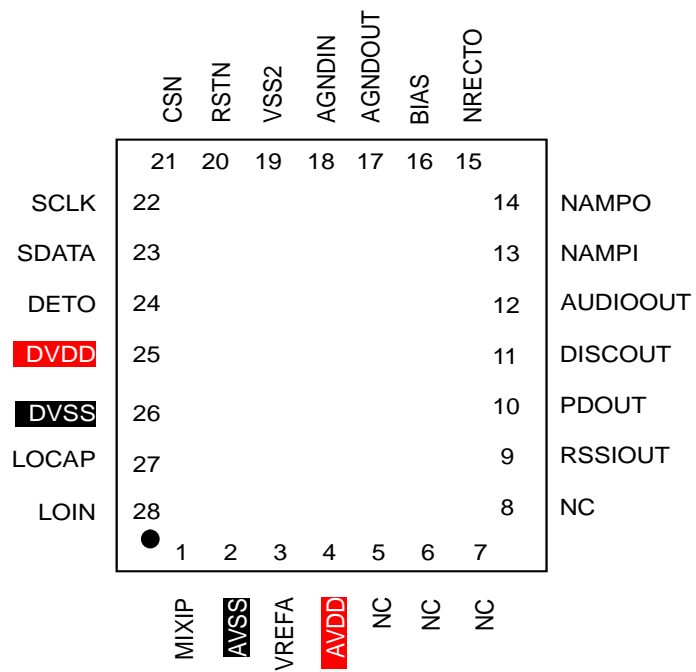| Package	Signal		Conditions at power down	Function
Pin No	Name	Type		
1	MIXIP	AI	Z	IF positive signal input pin
2	AVSS	PWR	-	Analog ground pin
3	VREFA	AI	H	Output pin to connect capacitor for LDO
4	AVDD	PWR	-	Analog VDD power supply pin
5	NC	AIO	Z	NC pin
6	NC	AIO	Z	NC pin
7	NC	AIO	Z	NC pin
8	NC	AIO	Z	NC pin
9	RSSIOUT	AO	Z	Output pin to connect capacitor for Received Signal Strength Indicator(RSSI)
10	PDOUT	AO	Z	Pin1 for DISCRIMINATOR Low-pass filter
11	DISCOUT	AO	Z	PIN2 for DISCRIMINATOR Low-pass filter
12	AUDIOOUT	AO	Z	Demodulated audio signal output pin
13	NAMPI	AI	Z	Input pin for noise squelch amplifier
14	NAMPO	AO	Z	Output pin for noise squelch amplifier
15	NRECTO	AI	Z	Output pin for the rectification circuit
16	BIAS	AO	Z	Output pin to connect bias resistor for reference voltage
17	AGNDOUT	AO	Z	Analog ground output pin. Connect the capacitor to stabilize the analog ground level.
18	AGNDIN	AI	Z	Analog ground input pin. Connect the capacitor to stabilize the analog ground level.
19	VSS2	PWR	-	VSS power supply pin. Normally supply 0V to this pin.
20	RSTN	DI	Z	Hardware reset pin
21	CSN	DI	Z	Chip select input pin for serial data
22	SCLK	DI	Z	Clock input pin for serial data
23	SDATA	DB	-	Input and output pin for serial data
24	DETO	DO	Z	Signal detect output pin
25	DVDD	PWR	-	Digital VDD power supply pin.
26	DVSS	PWR	-	Digital ground pin
27	LOCAP	AI	Z	Local signal input pin
28	LOIN	AI	Z	Local signal input pin

Note:
A: Analog, **D**: Digital, **PWR**: Power, **I**: Input, **O**: Output, **B**: Bidirectional, **Z**: High-Z, **L**: Low

When you use AK2364 in AVDD=2.6 to 3.6V operation, VREFA pin is connected to AVDD pin for power supplying. Please set LDO (Low Drop Out) power off setting.

When VREFA pin is supplied by external power supply, absolute maximum ratings and recommended operating conditions are based on AVDD level.

• Pin Assignment

```
                          CSN RSTN VSS2 AGNDIN AGNDOUT BIAS NRECTO
                           21  20   19   18    17    16   15

              SCLK  22                                        14   NAMPO
              SDATA 23                                        13   NAMPI
              DETO  24                                        12   AUDIOOUT
              DVDD  25                                        11   DISCOUT
              DVSS  26                                        10   PDOUT
              LOCAP 27                                         9   RSSIOUT
              LOIN  28                                         8   NC
                    ●
                     1    2    3    4    5    6    7

                   MIXIP AVSS VREFA AVDD NC  NC  NC
```

6. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	AVDD	-0.3	6.5	V
	DVDD	-0.3	6.5	V
Ground Level	VSS	0	0	V
Input Voltage	V_{IN} analog	-0.3	AVDD+0.3	V
	V_{IN} digital	-0.3	DVDD+0.3	V
Input Current (Except power supply pin)	I_{IN}	-10	+10	mA
Storage Temperature	T_{stg}	-55	130	°C

Note : All voltages are relative to the VSS pin.

Caution : Exceeding these maximum ratings can result in damage to the device.
Normal operation cannot be guaranteed under this extreme.

7. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Temperature	Ta		-40		85	°C
Power Supply Voltage	AVDD		2.6	3.0	5.5	V
	DVDD	DVDD ≤ AVDD	2.6	3.0	5.5	V
Analog Reference Voltage	AGND	LDO in use		1.35		V
		LDO not in use		1/2VDD		V
Output Load Resistance	R_L	AUDIOOUT, DISCOUNT, NAMPO	30			kΩ
Output Load Capacitance	C_L	AUDIOOUT, DISCOUNT, NAMPO			15	pF

Note : All voltages are relative to the VSS pin.

8. Digital DC Characteristics

| Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High level input voltage	V_{IH}	RSTN, SCLK, SDATA CSN	0.8DVDD			V
Low level input voltage	V_{IL}	RSTN, SCLK, SDATA CSN			0.2DVDD	V
High level input current	I_{IH}	VIH=DVDD RSTN, SCLK, SDATA CSN			10	uA
Low level input current	I_{IL}	VIL=0V RSTN, SCLK, SDATA CSN	-10			uA
High level output voltage	V_{OH}	IOH=+0.2mA SDATA	DVDD-0.4		DVDD	V
Low level output voltage	V_{OL}	IOL=-0.4mA SDATA, DETO	0.0		0.4	V

9. Digital AC Timing

1) Serial Interface Timing

AK2364 is connected to a CPU by three-wired interface through CSN, SCLK and SDATA pins, which can make reading and writing data for control registers.

Serial data named SDATA is consist of 1-bit read and write instruction(R/W), 6-bit address (A5 to A0) and 8-bit data (D7 to D0) in one frame.

Write mode
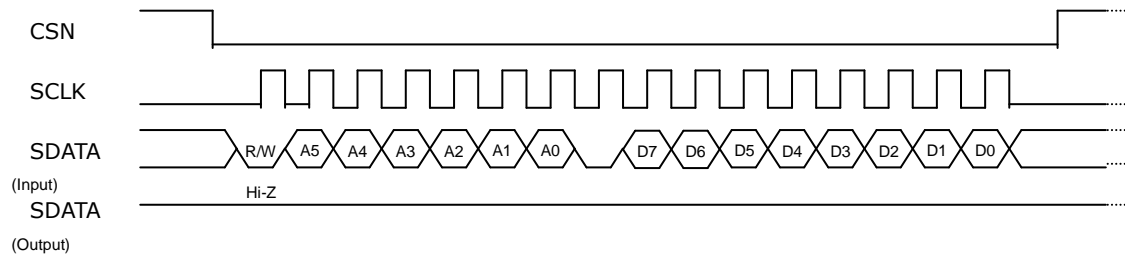
Read mode
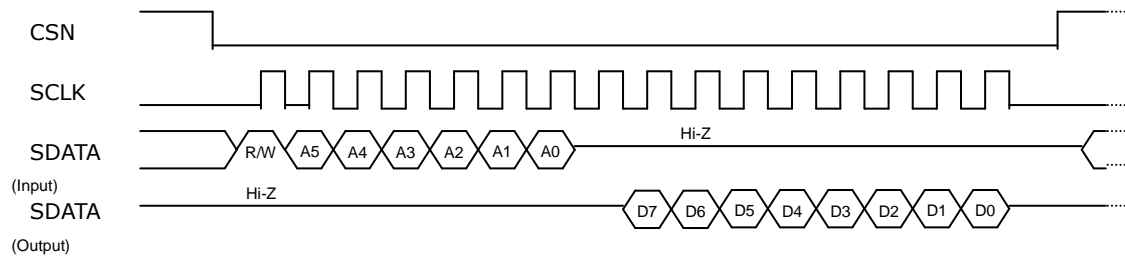
R/W : Instruction bit controls to write data to AK2364 or read back from it. When set to low, AK2364 is in write mode. When set to high, AK2364 is in read mode.

A5 to A0: Register address to be accessed.
D7 to D0: Write or read date to be accessed.

<1> CSN(Chip select) is normally selected high for disable.
When CSN is set to low, serial interface becomes active.

<2> In write mode, instruction, address and data input from SDATA pin are synchronized and latched with the rising edge of 16 iterations of SCLK clock. Set to low between address A0 and data D7.Input data is fixed synchronized with the rising edge of 16th clock. Note that if CSN become "H" before 16th clock, setting data becomes invalid. During the period when CSN is set to "L", consecutive writing is available.

<3> In read mode, instruction and address are synchronized and latched with the rising edge of 7 iterations of SCLK clock. And the register data are output from SDATA pin synchronized with the falling edge of 9 iterations of SCLK clock. The data between address A0 and data D7 is unstable. During the period when data is output, input to SDATA must be "Hi-z". Set CSN to "H" once reading is completed because consecutive reading is not valid.
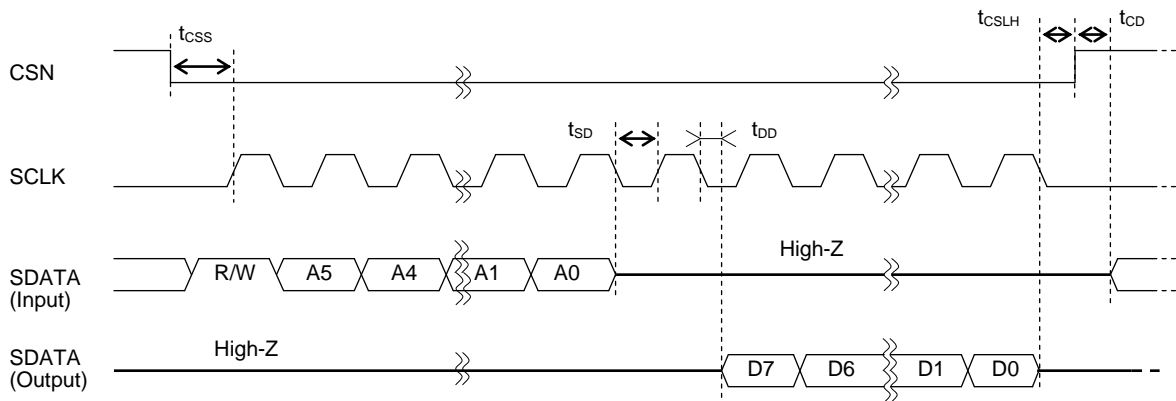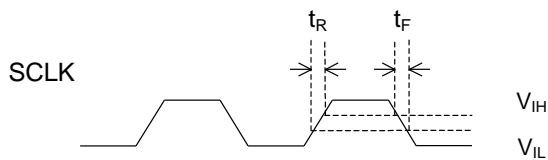
2) Detail Timing Chart

Write mode
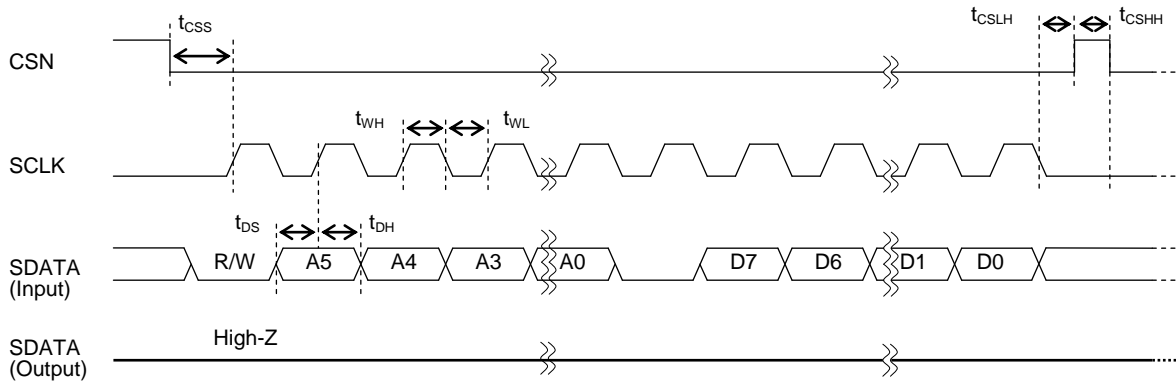

Read mode

Rising and falling time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSN setup time	t_{CSS}		100			ns
SDATA setup time	t_{DS}		100			ns
SDATA hold time	t_{DH}		100			ns
SCLK high time	t_{WH}		500			ns
SCLK low time	t_{WL}		500			ns
CSN low hold time	t_{CSLH}		100			ns
CSN high hold time	t_{CSHH}		100			ns
SDATA Hi-Z setup time	t_{SD}		500			ns
SCLK to SDATA output delay time	t_{DD}	20pF load			400	ns
CSN to SDATA input delay time	t_{CD}	20pF load	200			ns
SCLK rising time	t_R				250	ns
SCLK falling time	t_F				250	ns

Note: Digital input and output timing is relative to 0.5DVDD of rising signal and falling signal.

10. System Reset

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Hardware reset signal input width	t_{RSTN}	RSTN pin	1			us	*1)
Software reset		SRST register					*2)

*1) After power-on, be sure to perform a hardware reset operation (register initialization). The system is reset by a low pulse input of 1μs (min.) and enters the normal operation state. At this moment, the digital (DI) pins are set as follows: RSTN pin to high, SCLK pin to Low, SDATA pin to low, CSN pin to Low.
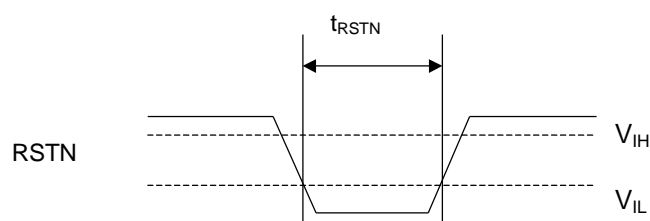
*2) When data 0x03:10101010 is written to the SRST[7:0] register, software reset is performed. This setting initializes the registers and the operation mode is set to mode 0 (power down). After software reset is completed, this register comes to "0".

11. Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Consumption Current	IDD0	Mode 0 Power down			10	μA
	IDD1	Mode 1 Standby, AGN DIN		0.1	0.2	mA
	IDD2	Mode 2 Standby, Lo buffer, VIREF		0.6	1.4	mA
	IDD3	Mode 3 When no input signal		7.0	10	mA

12. Analog Characteristics

For the following conditions unless otherwise specified: LOIN=50.4MHz,MIXIP=50.85MHz, Δf=±1.5kHz, fmod=1kHz、AGC+BPF=F4, the exposure back pad of the package is connected to VSS, with the external circuit shown in example page 21 to 24.

1) Local

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units	Notes
Local Frequency	F_{LO}	LOIN		45.9 50.4 57.6		MHz	
Input amplitude	V_{LO}	LOIN	0.2		1.0	V_{PP}	Note)

Note) Input from LOIN pin through DC cut

2) 2nd Mixer

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Input Impedance	Note)		50		Ω	Note)
Input Frequency			F_{LO} +0.45		MHz	
Voltage Gain			23		dB	
Noise Figure			13		dB	

Note) Include external matching circuit

3) Discriminator

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Demodulation Output Level	Δf=±3.0kHz,fmod=1kHz, LIMITER IN to AUDIOOUT Note)	60	100	140	mVrms	BAND =1
	Δf=±1.5kHz,fmod=1kHz, LIMITER IN to AUDIOOUT Note)	60	100	140	mVrms	BAND =0
S/N Ratio	Δf=±3.0kHz,fmod=1kHz, LIMITER IN to AUDIOOUT Note)		50		dB	BAND =1

Note) With De-emphasis＋BPF(0.3 to 3kHz)

4) RX Overall Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
12dB SINAD Input Sensitivity	Note)		-104		dBm	
IIP3			-16		dBm	
Demodulation Output Level	Δf=±3.0kHz,fmod=1kHz, AGC+BPF=F3 Note)	60	100	140	mVrms	BAND =1
	Δf=±1.5kHz,fmod=1kHz, AGC+BPF=F4 Note)	60	100	140	mVrms	BAND =0
S/N Ratio	Δf=±3.0kHz,fmod=1kHz, AGC+BPF=F3 Note)	40	46		dB	BAND =1
	Δf=±1.5kHz,fmod=1kHz, AGC+BPF=F4 Note)	34	40		dB	BAND =0

Note)With De-emphasis＋BPF(0.3 to3kHz)

5) RSSI Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
RSSI Output Voltage	MIXIP --> RSSIOUT MIXIP=-100dBm Input	0.1	0.36	0.62	V	
	MIXIP --> RSSIOUT MIXIP=-30dBm Input	1.4	2.0	2.6	V	

RSSI Characteristics
(VDD=3V)
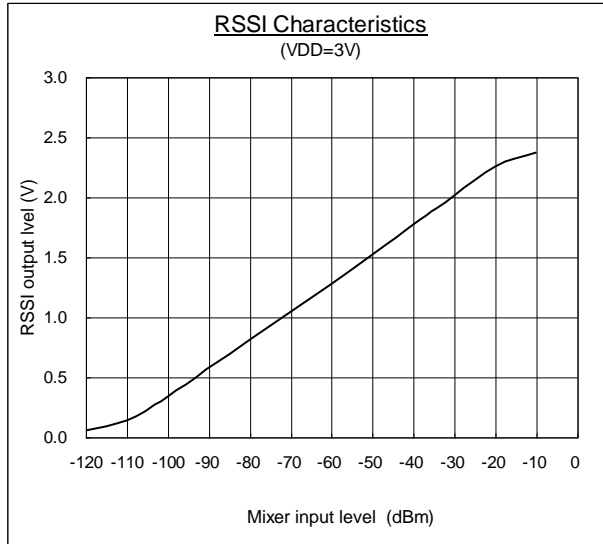
6) Noise Squelch Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Noise Detect Level	NRECTO --> DETO Detect High		0.5	0.7	V	
	NRECTO --> DETO Detect Low	0.3	0.4		V	
Noise Detect Characteristic	NAMPI --> NRECTO Input: 31kHz, 0.1mVrms	0.1	0.26	0.36	V	
	NAMPI --> NRECTO Input: 31kHz, 0.25mVrms	0.4	0.65	0.8	V	

Noise Detect Characteristics
(VDD=3V, fin=31kHz)

7) AGC+BPF Characteristics
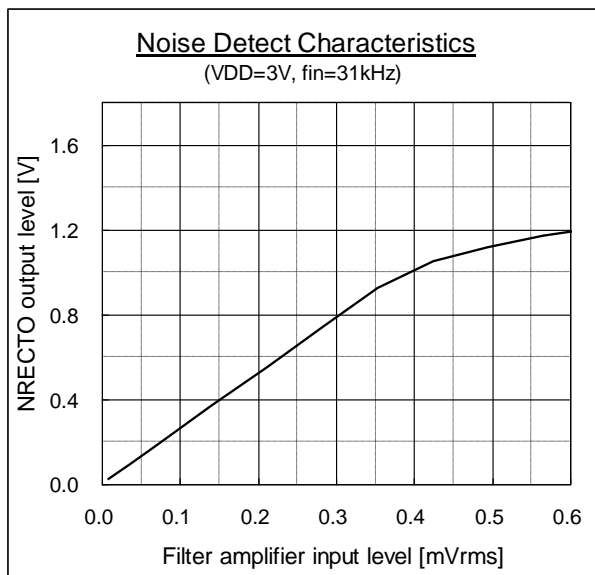
7.1) F1 (D type)

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Attenuation Characteristics (relative to the gain at 450kHz)	430kHz			-50	dB	
	440kHz	-6			dB	
	460kHz	-6			dB	
	470kHz			-50	dB	
Gain Ripple	Within 450±7kHz			3	dB	

7.2) F2 (E type)

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Attenuation Characteristics (relative to the gain at 450kHz)	435kHz			-50	dB	
	442.5kHz	-6			dB	
	457.5kHz	-6			dB	
	465kHz			-50	dB	
Gain Ripple	Within 450±5kHz			3	dB	

7.3) F3 (F type)

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Attenuation Characteristics (relative to the gain at 450kHz)	437.5kHz			-50	dB	
	444kHz	-6			dB	
	456kHz	-6			dB	
	462.5kHz			-50	dB	
Gain Ripple	Within 450±4kHz			3	dB	

7.4) F4 (G type)

Parameter	Condition	Min.	Typ.	Max.	Units	Notes
Attenuation Characteristics (relative to the gain at 450kHz)	439kHz			-50	dB	
	445.5kHz	-6			dB	
	454.5kHz	-6			dB	
	461kHz			-50	dB	
Gain Ripple	Within 450±3kHz			3	dB	

BPF F1 (BW=±10kHz)

BPF F2 (BW=±7.5kHz)

BPF F3 (BW=±6kHz)

BPF F4 (BW=±4.5kHz)
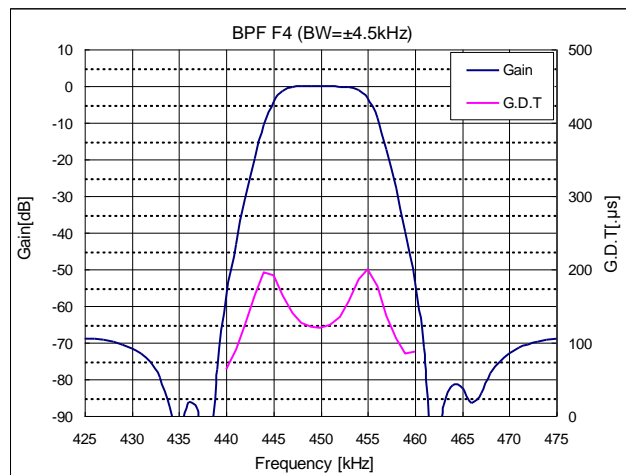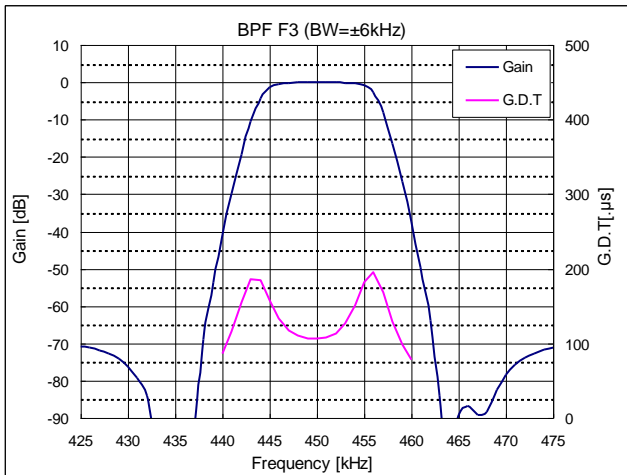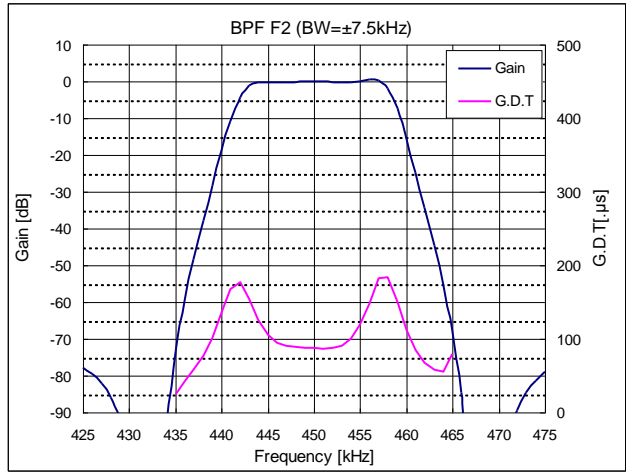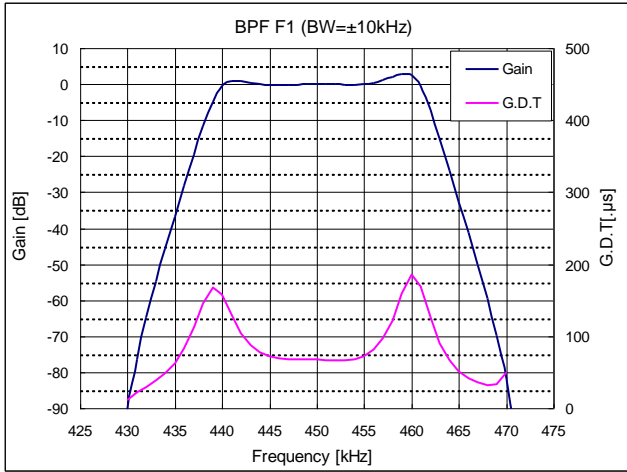
13. Serial Interface Configuration

1) Register Configuration

Name	ADRS	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)	W/R
Control register 1	0x01	LDOSTAT	PDLDON	BPF_BW[1:0]		LOFREQ[1:0]		BS[1:0]		W/R
		1	0	0	0	0	1	0	1	
Control register 2	0x02	Reserved			AGC_TIME[1:0]		AGC0_STEP	BAND	CAL	W/R
		0	0	0	0	0	1	0	0	
Software-reset	0x03	SRST[7:0]								W
		—	—	—	—	—	—	—	—	

Note: Do not access the data except specified address above.

2) Description of registers

Address 0x01 (Control Register 1)

Name	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Control Register 1	LDOSTAT	PDLDON	BPF_BW[1:0]		LOFREQ[1:0]		BS[1:0]	
Initial Value	1	0	0	0	0	1	0	1

LDO setting

Data	Function	Operation		Notes
		0	1	
LDO STAT	Output status In LDO power down	AVSS shorted	AVDD shorted	
PDLDON	LDO power control	OFF	ON	

BPF band width setting

BPF_BW [1]	BPF_BW [0]	name	6dB attenuation
0	1	F1	±10kHz
0	0	F2	±7.5kHz
1	0	F3	±6kHz
1	1	F4	±4.5kHz

Local frequency setting

LOFREQ [1]	LOFREQ [0]	Local frequency
0	0	45.9MHz
0	1	50.4MHz
1	0	57.6MHz

Note: Do no set the combination of the code which is not defined in the table given above.

Operation mode setting

BS[1]	BS[0]	Mode name	AGNDIN	VIREF system	Circuits except AGNDIN, LOBUF,VIREF
0	0	Mode0(Power-down)	OFF	OFF	OFF
0	1	Mode1(standby)	ON	OFF	OFF
1	0	Mode2	ON	ON	OFF
1	1	Mode3	ON	ON	ON

Address 0x02 (Control Register 2)

Name	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Control Register 2	Reserved			AGC_TIME[1:0]		AGC0_STEP	BAND	CAL
Initial Value	0	0	0	0	0	1	0	0

AGC_TIME[1:0] : AGC response time setting
This register set response time for AGC0 gain and AGC1 gain to change by 1step.

AGC_TIME [1]	AGC_TIME [0]	AGC response time [ms]					
		AGC0_STEP=0 setting			AGC0_STEP=1 setting		
		State A	State B	State C	State A	State B	State C
0	0	0.56	8.50	8.50	0.38	4.35	4.35
0	1	0.92	8.79	8.79	0.56	4.50	4.50
1	0	1.64	9.37	9.37	0.93	4.79	4.79
1	1	3.08	10.52	10.52	1.66	5.38	5.38

Note: Values above indicate response time during AGC gain changes from maximum to minimum or from minimum to maximum.
Note: AGC response time differs according to the following states.

State A: AGC0 output level is beyond the upper limit.
State B: AGC0 output level is within the upper limit and AGC1 output level is beyond the upper limit.
State C: AGC1 output level is under the lower limit.

Data	Function	Operation		Notes
		0	1	
AGC0_STEP	AGC0 gain switching range setting	±1dB	±2dB	
BAND	Demodulated signal level setting (Note1)	NARROW	WIDE	
CAL	Discriminator circuit calibration start trigger (Note2)	Invalid	Start	

Note1: When {BAND} register is set to "0", demodulated signal level at AUDIOOUT pin, when input signal is $\Delta f=\pm1.5$kHz dev, is 100mVrms typ. When {BAND} register is set to "1", demodulated signal level at AUDIOOUT pin, when input signal is $\Delta f=\pm3.0$kHz dev, is 100mVrms typ.

Note2: calibration is performed synchronized with the rising edge of {CAL}. After calibration is completed, this register is set to "0" automatically. It takes 1.3ms before calibration is completed. Refer to "calibration procedure" for further information.

Address 0x03 (Software Reset)

Name	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Software-reset	SRST[7:0]							
Initial Value	—	—	—	—	—	—	—	—

When data 0x03:10101010 is written to the SRST[7:0] register, software reset is performed.
Refer to System Reset for further information.

14. Calibration Procedure

1) AVDD=2.6 to 3.6V operation
   When you use AK2364 in AVDD=2.6 to 3.6V operation, VREFA pin is connected to AVDD pin for power supplying. Please set LDO (Low Drop Out) power off setting. Refer to 4-1) in page 22.

   AK2364 employs a function to calibrate free-running frequency of VCO in Discriminator and demodulated signal level. Before starting RX Operation, calibration is required in order to acquire proper VCO operation range and demodulated signal level.

Following procedure is required before calibration in LDO power off setting.

<1> Start up the external TCXO and continuously supply LO signal to AK2364.
<2> Set "11" to 0x01 {BS[1:0]} and start up all circuits. After this operation, the circuits necessary for calibration (LOBUF, VIREF and Discriminator) will be powered on and calibration can be possible in 500us.
<3> Calibration is begun by setting "1" to address 0x02 {CAL}. When the calibration is executed once, the calibration operation cannot be stopped excluding master reset. Even if "0" is written in {CAL}, the calibration is completely executed.
<4> Calibration data is maintained excluding the time when the master reset is executed or DVDD power supply is down.
<5> It takes 1.5ms for Discriminator to become steady after the calibration is completed.

Power-up sequence recommendation
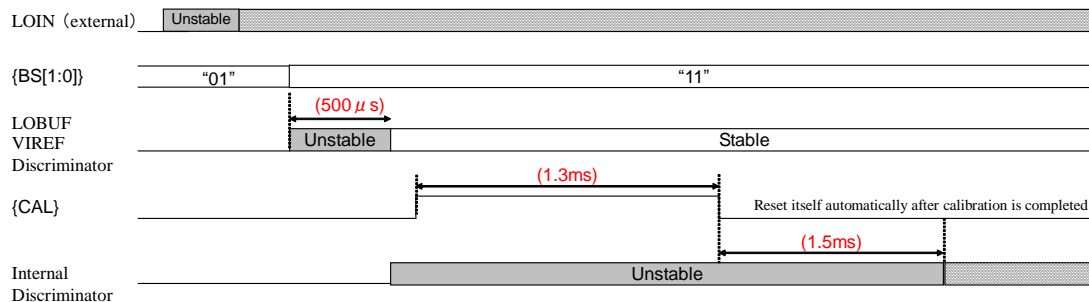
2) AVDD=3.6 to 5.5V operation
     When you use AK2364 in AVDD=3.6 to 5.5V operation, please set LDO power on setting.
     Refer to 4-2) in page 23.

Following procedure is required before calibration in LDO power on setting.

   <1> Start up the external TCXO and continuously supply LO signal to AK2364.
   <2> Set "10" to 0x01 {BS[1:0]} and start up VIREF circuits. This makes LDO set power up standby.
   <3> Set "0" to 0x01 {LDOSTAT} and LDO output shortened VSS once. This makes LDO power up
        time shortly.
   <4> Set "1" to 0x01 {LDOSTAT} and "1" to 0x01 {PDLDON}, then LDO power is on. It takes 130ms
        for AGNDIN pin output voltage to become stable.
   <5> Set "11" to 0x01 {BS[1:0]} and start up all circuits. After this operation, the circuits necessary for
        calibration (LOBUF,VIREF and Discriminator) will be powered on and calibration can be
        possible in 500us.
   <6> Calibration is begun by setting "1" to address 0x02 {CAL}. When the calibration is executed
        once, the calibration operation cannot be stopped excluding master reset. Even if "0" is written
        in {CAL}, the calibration is completely executed.
   <7> Calibration data is maintained excluding the time when the master reset is executed or DVDD
        power supply is down.
   <8> It takes 1.5ms for Discriminator to become stable after the calibration is completed.

Power-up sequence recommendation

LOIN（External）	Unstable
{BS[1:0]}	"01"	"10"	"11"
{LDOSTAT}	(100μs) (50μs)
{PDLDON}	(130ms)
AGNDIN	Unstable	Stable
LOBUF VIREF Discriminator	(500μs) Unstable	Stable
{CAL}	Reset itself automatically after calibration is completed	(1.3ms)
Internal Discriminator	(1.5ms) Unstable
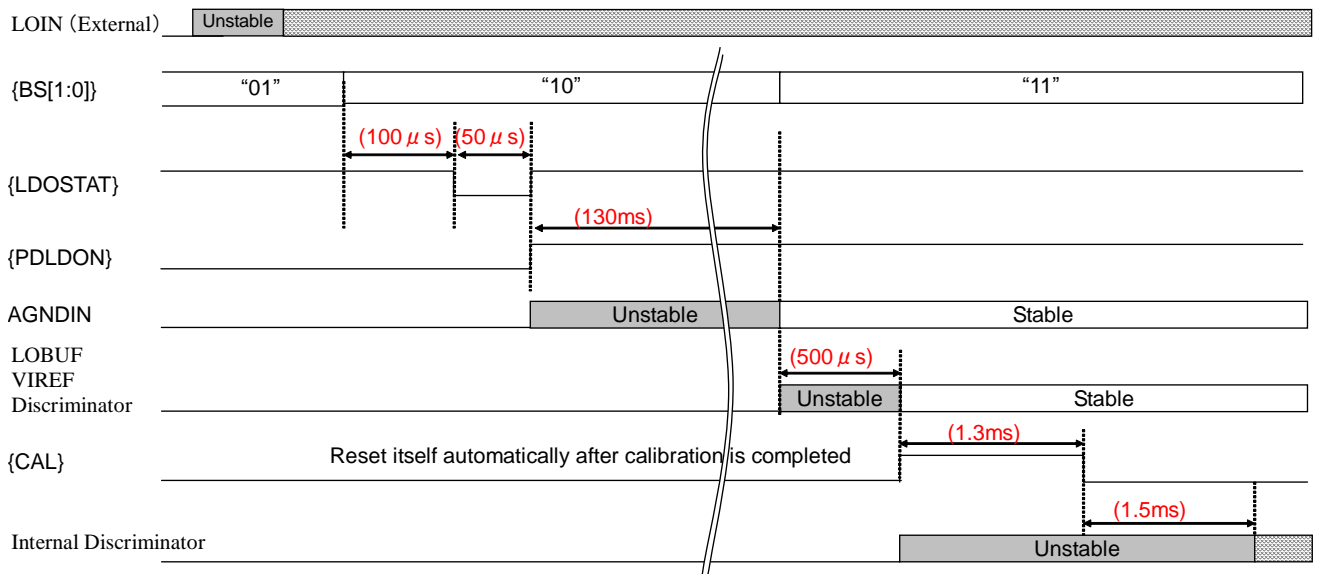
 Note: These values refer to the following recommended external application circuits.

15. Recommended External Application Circuits

1) Power supply stabilizing capacitors
   Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.

C1=0.1μF (Ceramic cap)

C2=10μF (Electrolytic cap)
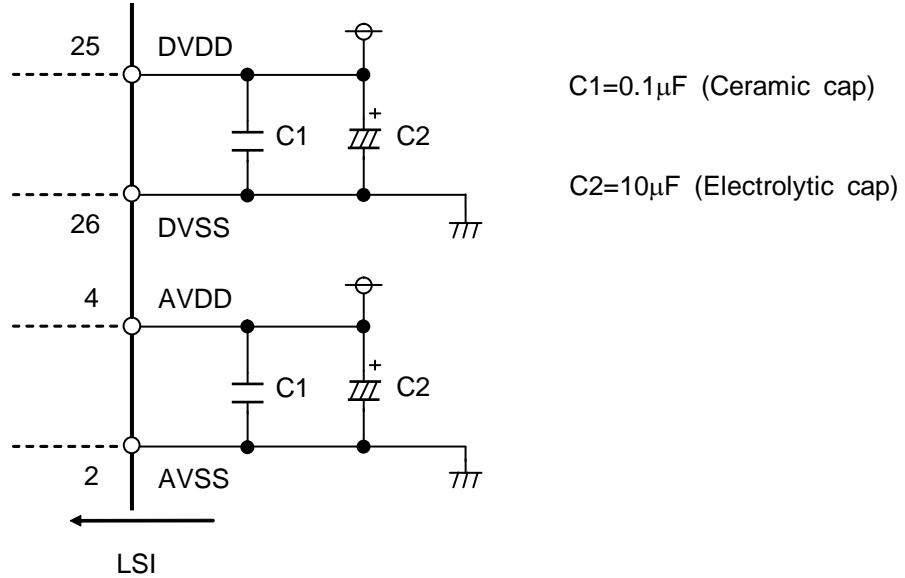
2) AGND stabilizing capacitors
   It is recommended that capacitors with 1μF or lager be connected between VSS and the AGND and AGNDIN pins to stabilize the AGND signal. The capacitors must be placed as close to the pins as possible.

C1=1μF (Electrolytic capacitor)

3) BIAS

R1=47kΩ±1%
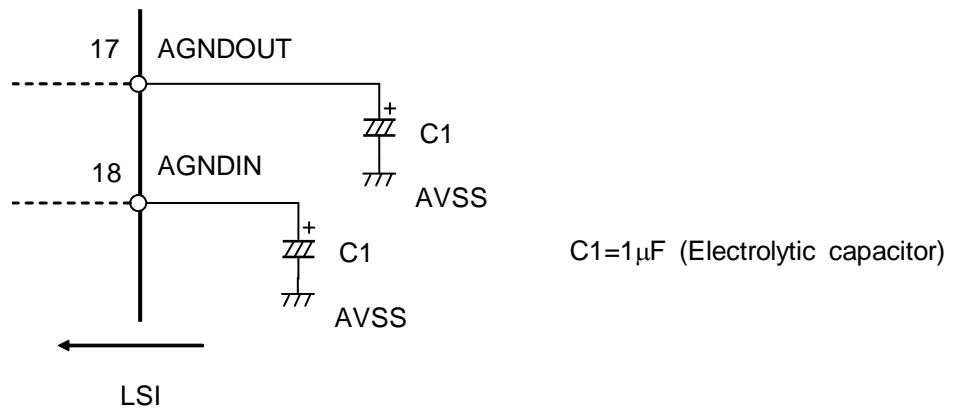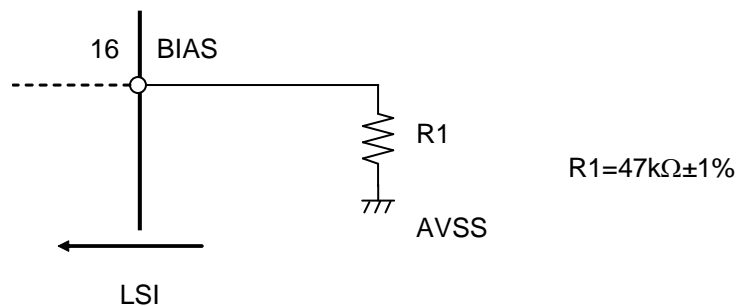
4-1) VREFA (AVDD=2.6 to 3.6V operation)

```
  3  │ VREFA
─ ─ ─○──────────────┐
  4  │ AVDD         │
─ ─ ─○──────────────┘
     │
     ←───────┐
     LSI
```
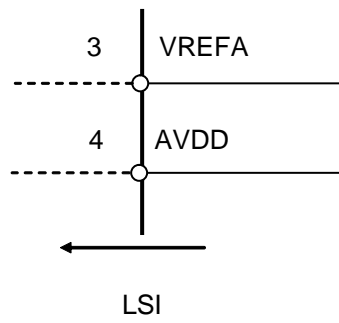
4-2) VREFA (AVDD=3.6 to 5.5V operation)

```
  3  │ VREFA
─ ─ ─○──────┬
     │      ═╪═ C1        C1=220nF
     ←──┐    ⏚
     LSI   AVSS
```

5) MIX

```
  1  │ MIXIP           C1   IF_INPUT
─ ─ ─○──╫──┬────┬──╫──○
     │ C2  R1⊰  §L1        C1=18pF, L1=470nF for 46.35MHz
     │      └────┘         C1=15pF, L1=470nF for 50.85MHz
     │        ⏚           C1=12pF, L1=390nF for 58.05MHz
     ←──┐
     LSI                   C2=10nF

                           R1=2.4kΩ
```

6) LOIN

```
  28 │ LOIN           LO_INPUT
─ ─ ─○──╫──────────○
     │ C1
     │ C2
─ ─ ─○──╫───┬          C1=C2=100pF
  27 │ LOCAP ⏚
     │      AVSS
     ←──┐
     LSI
```
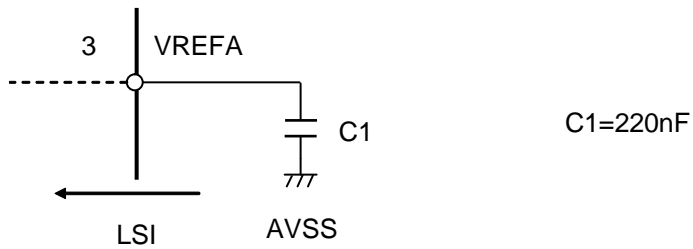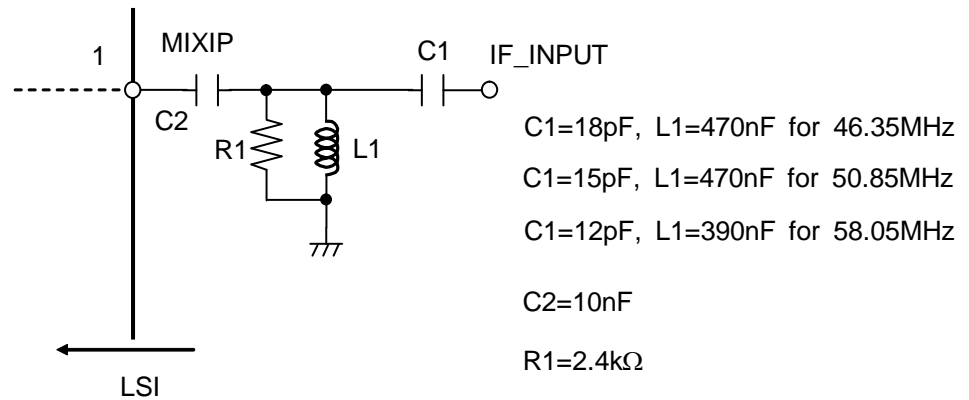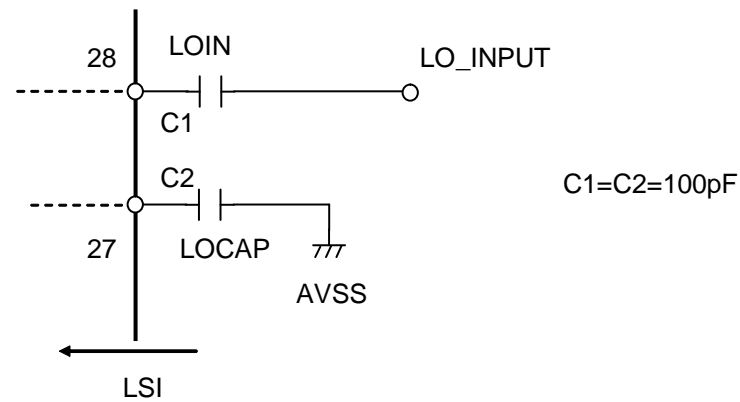
7) Discriminator
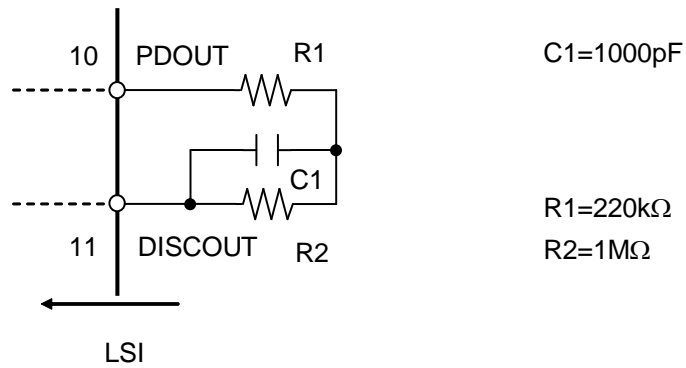
8) Noise AMP
The following gives a sample configuration of a BPF when input frequency is 31 kHz.
Some parameters can be calculated using following (1) to (3) equations.
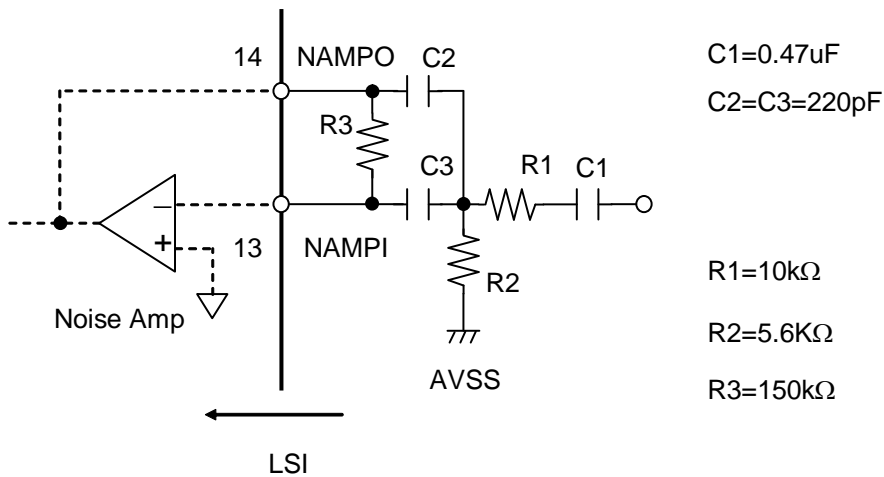
$$(1) \quad f_0 = \frac{1}{2\pi\sqrt{R_3(R_1 /\!/ R_2)C^2}}$$

$$(2) \quad G_v = \frac{R_3}{2R_1}$$

$$(3) \quad Q^2 = \frac{R_3}{4(R_1 /\!/ R_2)}$$

9) NECTO
   Rise time of noise detection is proportionate to C1=0.1uF and internal resistance 75kΩ

15 NRECTO

C1

C1=0.1μF

LSI   AVSS

10) RSSIOUT

9 RSSIOUT

C1   R1

R1=51kΩ
C1=1000pF

LSI   AVSS

11) DETO

DVDD

24 DETO   R1

R1=100kΩ

LSI
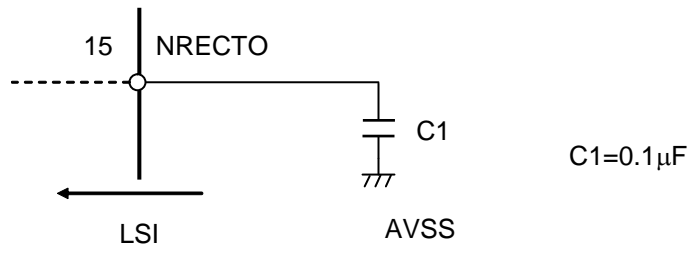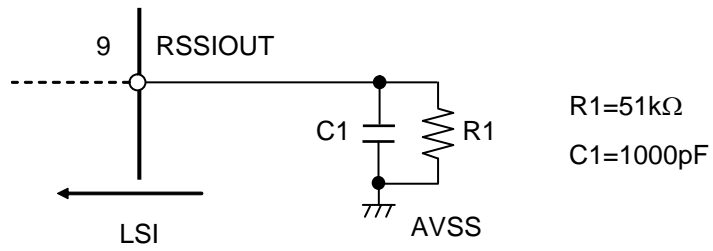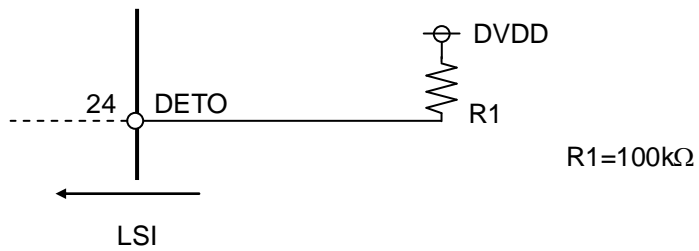
16. Packaging

□ Marking

2364
YWWL

●
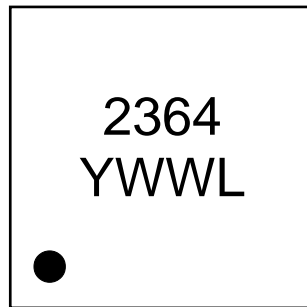
［Contents of YWWL］
Y： Last digit of calendar year. (Year 2011->1, 2012->2)

WW: Manufacturing week number.

L: Lot identification, given to each product lot which is made in a week.
LOT ID is given in alphabetical order (A, B, C…).

□ Mechanical Outline
Package：28pin QFN (4.0 x 4.0 x 0.7mm, 0.4mm pitch)
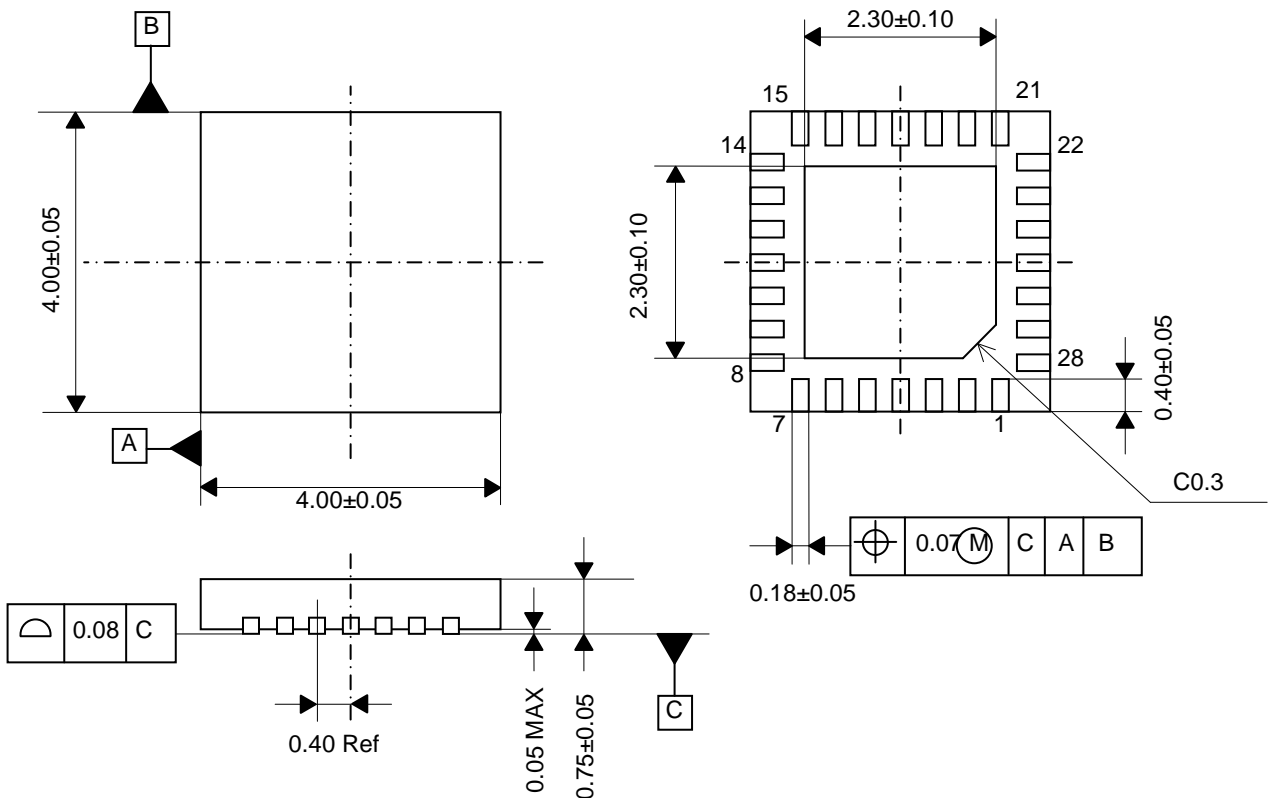
Note）The exposure pad(Exposed Pad）of the center of the package back is connected to opening
or VSS.

17. Important Notice

●Related Parts

Part#	Discription	Comments
Mixer		
AK1220	100MHz~900MHz High Linearity Down Conversion Mixer	IIP3:+22dBm
AK1222	100MHz~900MHz Low Power Down Conversion Mixer	IDD:2.9mA
AK1224	100MHz~900MHz Low Noise, High Liniarity Down Conversion Mixer	NF:8.5dB, IIP3:+18dBm
AK1228	10MHz~2GHz Up/Down Conversion Mixer	3V Supply, NF:8.5dB
AK1221	0.7GHz~3.5GHz High Linearity Down Conversion Mixer	IIP3:+25dBm
AK1223	3GHz~8.5GHz High Linearity Down Conversion Mixer	IIP3:+13dB, NF:15dB
PLL Synthesizer		
AK1541	20MHz~600MHz Low Power Fractional-N Synthesizer	IDD:4.6mA
AK1542A	20MHz~600MHz Low Power Integer-N Synthesizer	IDD:2.2mA
AK1543	400MHz~1.3GHz Low Power Fractional-N Synthesizer	IDD:5.1mA
AK1544	400MHz~1.3GHz Low Power Integer-N Synthesizer	IDD:2.8mA
AK1590	60MHz~1GHz Fractional-N Synthesizer	IDD:2.5mA
AK1545	0.5GHz~3.5GHz Integer-N Synthesizer	16-TSSOP
AK1546	0.5GHz~3GHz Low Phase Noise Integer-N Synthesizer	Normalized C/N:-226dBc/Hz
AK1547	0.5GHz~4GHz Integer-N Synthesizer	5V Supply
AK1548	1GHz~8GHz Low Phase Noise Integer-N Synthesizer	Normalized C/N:-226dBc/Hz
IFVGA		
AK1291	100~300MHz Analog Signal Control IF VGA w/ RSSI	Dynamic Range:30dB
integrated VCO		
AK1572	690MHz~4GHz Down Conversion Mixer with Frac.-N PLL and VCO	IIP3:24dBm, -111dBc/Hz@100kHz
AK1575	690MHz~4GHz Up Conversion Mixer with Frac.-N PLL and VCO	IIP3:24dBm, -111dBc/Hz@100kHz
IF Reciever (2nd Mixer + IF BPF + FM Detector)		
AK2364	Built-in programmable AGC+BPF, FM detector IC	IFBPF:±10kHz ~ ±4.5kHz
AK2365A	Built-in programmable AGC+BPF, IFIC	IFBPF:±7.5kHz ~ ±2kHz
Analog BB for PMR/LMR		
AK2345C	CTCSS Filter, Encoder, Decoder	24-VSOP
AK2360/ AK2360A	Inverted frequency(3.376kHz/3.020kHz) scrambler	8-SON
AK2363	MSK Modem/DTMF Receiver	24-QFN
AK2346B	0.3-2.55/3.0kHz Analog audio filter,	24-VSOP
AK2346A	Emphasis, Compandor, scrambler, MSK Modem	24-QFN
AK2347B	0.3-2.55/3.0kHz Analog audio filter	24-VSOP
AK2347A	Emphasis, Compandor, scrambler, CTCSS filter	24-QFN
Function IC		
AK2330	8-bit 8ch Electronic Volume	VREF can be selected for each channel
AK2331	8-bit 4ch Electronic Volume	VREF can be selected for each channel

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